REMARKS

Claims 1-20 are pending in the Application. Claims 8-20 are rejected under 35 U.S.C. §112, first paragraph. Claims 1-7 and 11-17 are rejected under 35 U.S.C. §102. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

Applicants thank the Examiner for discussing the Office Action with Applicants' Attorney on January 23, 2007.

I. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH:

The Examiner has rejected claims 8-20 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Office Action (11/1/2006), page 2. In particular, the Examiner asserts that the elements "a second and third tri-state inverters" in claim 8 were not described in the written description. *Id.* Applicants respectfully traverse.

Applicants kindly direct the Examiner's attention to at least page 4, line 19 – page 5, line 4 of Applicants' Specification which describes tri-state inverters 202, such as the claimed second tri-state inverter, coupled between a local bit line and a global bit line as illustrated in Figure 2. Applicants further direct the Examiner's attention to at least page 5, lines 5-17 of Applicants' Specification which describes tri-state inverter 305, such as the claimed third tri-state inverter, which is coupled between an output of latch 307 and the global bit line 303 as illustrated in Figure 3. Hence, Applicants' Specification describes the second and third tri-state inverters claimed in claim 8 in sufficient detail that one skilled in the art could reasonably conclude that the inventor had possession of the claimed invention. As a result, claims 8-10 are allowable under 35 U.S.C. §112, first paragraph. M.P.E.P. §2163.

Further, the Examiner states:

> Regarding claims 11-17, claimed invention including 'a transmission gate circuit.' As described in paragraph 0021 'the tri-state inverter 202 is replaced with transmission gate multiplexor circuit comprising transmission gate 220 and inverter 221.' Since 202 in Figure 2 is an inverter only, it not a multiplexor circuit. With understanding of

> examiner the function of a mux is different from function of an inverter, and 'the multiplexor 205 is replaced by a transmission gate multiplexor circuit comprising transmission gate 330 and inverter 331 in Figure 6.' As shown in Figure 5, the design of this embodiment is mux 205 is coupled from output of bit line, while the design of Figure 6 of present invention, transmission gate multiplexor circuit comprising transmission gate 330 and inverter 331 is input to bit line. Examiner does not understand how can replacing a mux 205 by transmission 330 and inverter 331, because they are not the same location and do difference function in design. In written description applicant discloses 'a transmission gate multiplexor' comprising transmission gate 330 and inverter 331. A 'transmission gate circuit' is not defined in specification. Office Action (11/1/2006), pages 2-3.

Applicants respectfully request the Examiner to clarify these statements pursuant to 37 C.F.R. §1.104(c)(2). Applicants do not understand the connection between the rejections of claims 11-17 under 35 U.S.C. §112, first paragraph, and all of the Examiner's above statements.

Based on Applicants' understanding of the above-indicated Examiner's statements, the Examiner believes that a "transmission gate circuit" in claim 11 is not defined in the Specification. Applicants respectfully traverse. Applicants kindly direct the Examiner's attention to at least page 5, line 29 – page 6, line 5 of Applicants' Specification which describes a transmission gate multiplexor circuit, such as the claimed transmission gate circuit, which is coupled between an output of latch 307 and bit line 303 as illustrated in Figure 6. Hence, Applicants' Specification describes the transmission gate circuit claimed in claim 11 in sufficient detail that one skilled in the art could reasonably conclude that the inventor had possession of the claimed invention. As a result, claims 11-17 are allowable under 35 U.S.C. §112, first paragraph. M.P.E.P. §2163.

Further, based on Applicants' understanding of the above-indicated Examiner's statements, the Examiner appears to be asserting that element 202 in Figure 2 of Applicants' Specification is not a multiplexor circuit. Applicants agree with the Examiner's statement. However, Applicants do not understand why the Examiner mentions this point.

Further, the Examiner points out the differences between Figures 5 and 6 of Applicants' Specification. Office Action (11/1/2006), pages 2-3. As illustrated in Figures 5 and 6 and described in Applicants' Specification, multiplexor 205 is replaced by multiplexor circuit including transmission gate 330 and inverter 331. The multiplexor circuit is coupled between the output of latch 307 and global bit line 303. By having such an arrangement, the register file of Figure 6 performs the same operation as that of Figure 5 without the delay associated with multiplexor 205. (See, e.g., page 5, lines 5-17 and page 5, line 29 – page 6, line 5 of Specification). Hence, Applicants' Specification describes the transmission gate circuit claimed in claim 11 in sufficient detail that one skilled in the art could reasonably conclude that the inventor had possession of the claimed invention. As a result, claims 11-17 are allowable under 35 U.S.C. §112, first paragraph. M.P.E.P. §2163.

Further, the Examiner asserts that the limitation of "wherein a multiplexor is not coupled between the bit line and the latch" as recited in claims 7 and 17 is not a claimed invention. Office Action (11/1/2006), page 3. Applicants respectfully assert that this not an appropriate ground of rejection for allegedly failing to comply with the written description requirement under 35 U.S.C. §112, first paragraph. The function of the written description requirement is to ensure that the inventor had possession of, as of the filing date of the application relied on, the specific subject matter later claimed by him or her; how the specification accomplishes this is not material. *In re Herschler*, 591 F.2d 693, 700-01, 200 U.S.P.Q. 711, 717 (C.C.P.A. 1979); M.P.E.P. §2161.

Further, Applicants respectfully assert that the claim limitation of claims 7 and 17 is a proper claim limitation. The Examiner has not provided any evidence as to why this claim limitation is not a proper claim limitation. Applicants respectfully request the Examiner to particularly point out the rationale as to why the claim limitation of claims 7 and 17 is not a proper claim limitation pursuant to 37 C.F.R. §1.104(c)(2).

Additionally, the Examiner asserts that "transmission gate," as recited in claim 18 is not defined in the written description. Office Action (11/1/2006), page 3.

Applicants kindly direct the Examiner's attention to at least page 5, line 29 – page 6, line 5 of Applicants' Specification which describes transmission gates 220 and 330, as illustrated in Figures 5 and 6. Hence, Applicants' Specification describes transmission gates in sufficient detail that one skilled in the art could reasonably conclude that the inventor had possession of the claimed invention. As a result, claims 18-20 are allowable under 35 U.S.C. §112, first paragraph. M.P.E.P. §2163.

II. REJECTIONS UNDER 35 U.S.C. §102(a)/(b)/(e):

The Examiner has rejected claims 1-6 and 11-16 under 35 U.S.C. §102(a) as being anticipated by Applicants' Admitted Prior Art (hereinafter "AAPA"). The Examiner has further rejected claims 1-7 and 11-17 under 35 U.S.C. §102(e) as being anticipated by Chu et al. (Patent Application Publication No. 2005/0099851) (hereinafter "Chu"). The Examiner has further rejected claims 1-7 and 11-17 under 35 U.S.C. §102(b) as being anticipated by Henkels et al. (U.S. Patent No. 5,481,495) (hereinafter "Henkels"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

A. Claims 1-6 and 11-16 are not anticipated by AAPA.

Applicants respectfully assert that AAPA does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 1. The Examiner cites element 204 in Figures 2 and 5 of Applicants' Specification as disclosing the above-cited claim limitation. Office Action (11/1/2006), page 4. Applicants respectfully traverse and assert that AAPA instead discloses that inverter 204 is coupled between a bit line and the input of a multiplexor 205. Inverter 204 is not coupled between an output of the latch and the bit line. Hence, APPA does not disclose all of the limitations of claim 1, and thus AAPA does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that AAPA does not disclose "a transmission gate circuit coupled between an output of the latch and the bit line" as recited in claim 11. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 11. M.P.E.P. §2131.

Claims 2-6 each recite combinations of features of independent claim 1 and hence claims 2-6 are not anticipated by AAPA for at least the above-stated reasons that claim 1 is not anticipated by AAPA. Claims 12-16 each recite combinations of features of independent claim 11 and hence claims 12-16 are not anticipated by AAPA for at least the above-stated reasons that claim 11 is not anticipated by AAPA.

Claims 2-6 and 12-16 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by AAPA.

For example, AAPA does not disclose "another inverter coupled between the bit line and an input of the latch" as recited in claim 2. The Examiner cites element 202 of Applicants' Specification as disclosing the above-cited claim limitation. Office Action (11/1/2006), page 4. Applicants respectfully traverse and assert that element 202 corresponds to tri-state inverters coupled between local bit line 201 and global bit line 203. Applicants' Specification, page 4, line 19 – page 5, line 4; Figure 2. Tri-state inverters 202 are not coupled between the bit line (Examiner had previously asserted that global bit line 203 discloses the bit line claimed) and an input of the latch coupled to the bit line. Hence, APPA does not disclose all of the limitations of claim 2, and thus AAPA does not anticipate claim 2. M.P.E.P. §2131.

Applicants further assert that AAPA does not disclose "wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter" as recited in claim 4. The Examiner had previously cited element 204 of Applicants' Specification as disclosing the inverter claimed. Office Action (11/1/2006), page 4.

The Examiner is now citing element 202 of Applicants' Specification as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse. The Examiner cannot cite two separate and distinct elements (202 and 204) as disclosing the same claimed inverter. As illustrated in Figure 2 of Applicants' Specification, inverter 204 is not a tri-state inverter. Further, if the Examiner intends on using element 202 of Applicants' Specification as disclosing the claimed inverter, then Applicants respectfully point out that inverter 202, as illustrated in Figure 2, is not coupled between an output of the latch and the bit line as required in claim 1. Hence, APPA does not disclose all of the limitations of claim 4, and thus AAPA does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that AAPA does not disclose "wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch" as recited in claim 5. The Examiner cites element 202 as disclosing such an inverter. Office Action (11/1/2006), page 4. The Examiner had previously cited element 204 of Applicants' Specification as disclosing the inverter claimed. *Id.* Applicants respectfully traverse. The Examiner cannot cite two separate and distinct elements (202 and 204) as disclosing the same claimed inverter. As illustrated in Figure 2 of Applicants' Specification, inverter 204 does not have its output coupled to the bit line (Examiner asserts that global bit line 203 discloses the bit line) and have its input coupled to the output of the latch (Examiner assets that element 207 corresponds to the claimed latch). Further, as illustrated in Figure 2 of Applicants' Specification, inverter 202 does not have its input coupled to the output of the latch (Examiner assets that element 207 corresponds to the claimed latch). Hence, APPA does not disclose all of the limitations of claim 5, and thus AAPA does not anticipate claim 5. M.P.E.P. §2131.

Applicants further assert that AAPA does not disclose "an inverter coupled between the bit line and an input of the latch" as recited in claim 12. Applicants further assert that AAPA does not disclose "wherein the transmission gate circuit receives a hold select signal" as recited in claim 14. Applicants further assert that AAPA does not disclose "wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled

to the output of the latch" as recited in claim 15. The Examiner has not specifically addressed these limitations. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed these limitations, the Examiner has not established a *prima facie* case of anticipation in rejecting claims 12, 14 and 15. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within AAPA, and thus claims 1-6 and 11-16 are not anticipated by AAPA. M.P.E.P. §2131.

B. Claims 1-7 and 11-17 are not anticipated by Chu.

Applicants respectfully assert that Chu does not disclose "a plurality of register file cells coupled to a bit line" as recited in claim 1 and similarly in claim 11. The Examiner has not addressed all the elements in this limitation. Applicants kindly request the Examiner to particularly point out in Chu where Chu discloses a bit line coupled to the plurality of register file cells pursuant to 37 C.F.R. §1.104(c)(2). Thus, Chu does not disclose all of the limitations of claims 1 and 11, and thus Chu does not anticipate claims 1 and 11. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "a latch coupled to the bit line" as recited in claim 1 and similarly in claim 11. The Examiner cites elements I1 and I2 in cell 124 in Figure 1E of Chu as disclosing the above-cited claim limitation. Office Action (11/1/2006), page 5. The Examiner had previously cited cell 124 of Chu as disclosing a plurality of register cells. *Id.* The Examiner has not addressed the limitation of a bit line. Applicants respectfully traverse the assertion that Chu discloses the above-cited claim limitation.

The Examiner cannot cite an element within cell 124 of Chu as disclosing a latch coupled to the bit line when the Examiner had previously cited cell 124 of Chu as disclosing a plurality of register file cells coupled to a bit line. The latch is a distinct different element from the plurality of register file cells. It is not a logical

claim interpretation to say element A (register file cells) is coupled to a bit line and then say, element B (latch within register file cells), which is within element A, is coupled to the bit line. You are in essence making redundant statements. Since element A is coupled to the bit line, then obviously element B, which is within element A, is coupled to the bit line. It is clear, based on Applicants' Specification, that the latch is a distinct different element from the plurality of register file cells. The Examiner must cite an element distinct from the plurality of register file cells. The pending claims must be given their broadest reasonable interpretation consistent with the specification. *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2d 1664, 1667 (Fed. Cir. 2000); M.P.E.P. §2111. The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); M.P.E.P. §2111. Since the Examiner has not provided a reasonable interpretation consistent with the specification or consistent with the interpretation that those skilled in the art would reach, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1 and 11. M.P.E.P. §2111.

Applicants further assert that Chu does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 1. The Examiner cites element I0 in Figure 1C to disclose such an inverter. Office Action (11/1/2006), page 5. Applicants respectfully traverse.

As illustrated in Figure 1C, I0 corresponds to an inverter in selector 122. This inverter is not coupled between the output of the latch (Examiner asserts that elements I1, I2 in Figure 1E of Chu discloses the claimed latch) and the bit line. Applicants respectfully request the Examiner to particularly point out in Chu where Chu discloses the claimed bit line pursuant to 37 C.F.R. §1.104(c)(2). Thus, Chu does not disclose all of the limitations of claim 1, and thus Chu does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "a transmission gate circuit coupled between an output of the latch and the bit line" as recited in claim 11. The Examiner cites selector 122 of Chu as disclosing a transmission gate circuit.

Office Action (11/1/2006), page 5. The Examiner further cites elements 11, 12 in Figure 1E of Chu as disclosing the claimed latch. *Id.* The Examiner does not address where Chu discloses the bit line. Applicants respectfully traverse the assertion that Chu discloses the above-cited claim limitation.

Chu instead discloses that selector 122 has an NFET/PFET pair of transistors forming a transmission gate. [0010]. As illustrated in Figure 1C, this transmission gate is not coupled between an output of the latch formed by elements I1, 12 in Figure 1E and the bit line. Applicants respectfully request the Examiner to particularly point out in Chu where Chu discloses the claimed bit line pursuant to 37 C.F.R. §1.104(c)(2). Thus, Chu does not disclose all of the limitations of claim 11, and thus Chu does not anticipate claim 11. M.P.E.P. §2131.

Claims 2-7 each recite combinations of features of independent claim 1 and hence claims 2-7 are not anticipated by Chu for at least the above-stated reasons that claim 1 is not anticipated by Chu. Claims 12-17 each recite combinations of features of independent claim 11 and hence claims 12-17 are not anticipated by Chu for at least the above-stated reasons that claim 11 is not anticipated by Chu.

Claims 2-7 and 12-17 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Chu.

For example, Chu does not disclose "another inverter coupled between the bit line and an input of the latch" as recited in claim 2 and similarly in claim 12. The Examiner cites I3 in Figure 1E of Chu as disclosing the above-cited claim limitation. Office Action (11/1/2006), page 5. Applicants respectfully traverse.

As illustrated in Figure 1E of Chu, inverter 13 is coupled to the output of the memory latch formed by a pair of crossed coupled inverters 11 and 12 (Examiner asserts that inverters 11 and 12 disclose the claimed latch). [0006]. Hence, inverter 13 is not coupled to an input of the latch. Further, Applicants respectfully request the Examiner to particularly point out in Chu where Chu discloses the claimed bit line pursuant to 37 C.F.R. §1.104(c)(2). Thus, Chu does not disclose all of the limitations of claims 2 and 12, and thus Chu does not anticipate claims 2 and 12. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 3 and similarly in claim 13. The Examiner had previously cited inverters I1 and I2 of Figure 1E of Chu as disclosing the claimed latch. Office Action (11/1/2006), page 5. The Examiner further cites Figure 1E of Chu as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

As illustrated in Figure 1E of Chu, the output of inverters I1 and I2 is not the output of the register file (Examiner asserts that element 100 of Chu discloses the register file). Instead, as illustrated in Figure 1A, the output of static register-file bit-read circuit 100 is the RD_DATA_SEL signal which is outputted from inverter 130. Thus, Chu does not disclose all of the limitations of claims 3 and 13, and thus Chu does not anticipate claims 3 and 13. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter" as recited in claim 4. The Examiner cites element I0 in Figure 1C of Chu as disclosing the inverter and cites element SEL_0 in Figure 1C of Chu as disclosing the hold select signal. Office Action (11/1/2006), page 5. Applicants respectfully traverse.

As illustrated in Figure 1C, inverter I0 is not a tri-state inverter. Further, the signal SEL_0 is not a hold select signal. Instead, SEL_0 corresponds to the select line of a selector 122. [0010]. Thus, Chu does not disclose all of the limitations of claim 4, and thus Chu does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch" as recited in claim 5. The Examiner cites element I0 in Figure 1C of Chu as disclosing the inverter. Office Action (11/1/2006), page 5. The Examiner further cites inverters I1 and I2 in Figure 1E of Chu as disclosing the claimed latch. *Id.* Applicants respectfully traverse.

As illustrated in Figure 1C, the output of inverter I0 is not coupled to a bit line. Applicants respectfully request the Examiner to particularly point out in Chu where Chu discloses the claimed bit line pursuant to 37 C.F.R. §1.104(c)(2). Further,

as illustrated in Figure 1C, the input of inverter I0 is not coupled to the output of inverters I1 and I2 in Figure 1E. Instead, Figure 1C of Chu discloses that the input of inverter I0 is coupled to decoder 110 via a select line. [0010]. Thus, Chu does not disclose all of the limitations of claim 5, and thus Chu does not anticipate claim 5. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "wherein data is read out of the register array to be input into the latch" as recited in claim 6 and similarly in claim 16. The Examiner cites the signal WR_DATA in Figure 1E of Chu as disclosing data that is read out of the register array. Office Action (11/1/2006), page 5. The Examiner had previously cited element 100 of Chu as disclosing the register array. *Id.* The Examiner had further previously cited inverters I1 and I2 in Figure 1E of Chu as disclosing the claimed latch. *Id.* Applicants respectfully traverse the assertion that Chu discloses the above-cited claim limitation.

As illustrated in Figure 1E of Chu, the signal WR_DATA is clearly not read out of static register circuit 100 (Examiner asserts that register circuit 100 discloses the register array) to be input into inverters I1 and I2 (Examiner asserts that inverters I1 and I2 disclose the claimed latch). Hence, Chu does not disclose all of the limitations of claims 6 and 16, and thus Chu does not anticipate claims 6 and 16. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "wherein the transmission gate circuit receives a hold select signal" as recited in claim 14. The Examiner cites element SEL_0 in Figure 1C of Chu as disclosing the hold select signal. Office Action (11/1/2006), page 5. The Examiner further cites paragraph [0039] of Chu as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

As illustrated in Figure 1C, the signal SEL_0 is not a hold select signal. Instead, Chu discloses that signal SEL_0 corresponds to the select line of a selector 122. [0010]. Thus, Chu does not disclose all of the limitations of claim 14, and thus Chu does not anticipate claim 14. M.P.E.P. §2131.

Further, Chu instead discloses that during every address cycle one of the selectors 122 will be addressed, i.e., selected, and that selector will be one of the

selectors coupled to multiplexor output node READ_DATA_1 or else one of the selectors coupled to READ_DATA_2. [0039]. There is no language in the cited passage that discloses that the transmission gate (Examiner cites the transmission gate of selector 122 as disclosing the claimed transmission gate) receives a hold select signal. Thus, Chu does not disclose all of the limitations of claim 14, and thus Chu does not anticipate claim 14. M.P.E.P. §2131.

Applicants further assert that Chu does not disclose "wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled to the output of the latch" as recited in claim 15. The Examiner cites selector 122 as disclosing the claimed transmission gate circuit. Office Action (11/1/2006), page 5. The Examiner further cites inverters I1 and I2 as disclosing the claimed latch. *Id.* The Examiner further cites paragraph [0039] of Chu as disclosing the above-cited claim limitation. *Id.* at page 6. The Examiner has not addressed the claim limitation directed to a bit line. Applicants respectfully traverse the assertion that Chu discloses the above-cited claim limitation.

As illustrated in Figure 1C, the output of selector 122 is not coupled to a bit line. Applicants respectfully request the Examiner to particularly point out in Chu where Chu discloses the claimed bit line pursuant to 37 C.F.R. §1.104(c)(2). Thus, Chu does not disclose all of the limitations of claim 15, and thus Chu does not anticipate claim 15. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Chu, and thus claims 1-7 and 11-17 are not anticipated by Chu. M.P.E.P. §2131.

C. Claims 1-7 and 11-17 are not anticipated by Henkels.

Applicants respectfully assert that Henkels does not disclose "a latch coupled to the bit line" as recited in claim 1 and similarly in claim 11. The Examiner cites inverters 11 and 12 in Figure 1 of Henkels as disclosing the claimed latch coupled to the bit line. Office Action (11/1/2006), page 6. The Examiner had previously cited Figure 1 of Henkels as disclosing a plurality of register cells coupled to a bit line. *Id.*

Applicants respectfully traverse the assertion that Henkels discloses the above-cited claim limitation.

The Examiner cannot cite an element within the register file cell of Henkels as disclosing a latch coupled to the bit line when the Examiner had previously cited the register file cell of Henkels as disclosing a plurality of register file cells coupled to a bit line. The latch is a distinct different element from the plurality of register file cells. It is not a logical claim interpretation to say element A (register file cells) is coupled to a bit line and then say, element B (latch within register file cells), which is within element A, is coupled to the bit line. You are in essence making redundant statements. Since element A is coupled to the bit line, then obviously element B, which is within element A, is coupled to the bit line. It is clear, based on Applicants' Specification, that the latch is a distinct different element from the plurality of register file cells. The Examiner must cite an element distinct from the plurality of register file cells. The pending claims must be given their broadest reasonable interpretation consistent with the specification. *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2d 1664, 1667 (Fed. Cir. 2000); M.P.E.P. §2111. The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); M.P.E.P. §2111. Since the Examiner has not provided a reasonable interpretation consistent with the specification or consistent with the interpretation that those skilled in the art would reach, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1 and 11. M.P.E.P. §2111.

Applicants further assert that Henkels does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 1. The Examiner had previously cited inverters 11 and 12 in Figure 1 of Henkels as disclosing the claimed latch coupled to the bit line. Office Action (11/1/2006), page 6. Further, the Examiner had previously cited Figure 1 of Henkels as disclosing a plurality of register cells coupled to a bit line. *Id.* Further, the Examiner cites element 15 in Figure 1 of Henkels as disclosing such an inverter. *Id.* Applicants respectfully traverse.

Again, the Examiner cannot cite an element within the register file cell of Henkels as disclosing an inverter coupled between an output of the latch and the bit line when the Examiner had previously cited the register file cell of Henkels as disclosing a plurality of register file cells coupled to a bit line. The inverter and the latch are distinct different elements from the plurality of register file cells. It is not a logical claim interpretation to say element A (register file cells) is coupled to a bit line and then say, element B (latch within register file cells) and element C (an inverter within register file cells), which are within element A, is coupled to the bit line. You are in essence making redundant statements. Since element A is coupled to the bit line, then obviously elements B and C, which are within element A, are coupled to the bit line. It is clear, based on Applicants' Specification, that the latch and inverter are distinct different elements from the plurality of register file cells. The Examiner must cite elements distinct from the plurality of register file cells. The pending claims must be given their broadest reasonable interpretation consistent with the specification. *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2d 1664, 1667 (Fed. Cir. 2000); M.P.E.P. §2111. The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); M.P.E.P. §2111. Since the Examiner has not provided a reasonable interpretation consistent with the specification or consistent with the interpretation that those skilled in the art would reach, the Examiner has not presented a *prima facie* case of anticipation for rejecting claim 1. M.P.E.P. §2111.

Applicants further assert that Henkels does not disclose "a transmission gate circuit coupled between an output of the latch and the bit line" as recited in claim 11. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 11. M.P.E.P. §2131.

Claims 2-7 each recite combinations of features of independent claim 1 and hence claims 2-7 are not anticipated by Henkels for at least the above-stated reasons that claim 1 is not anticipated by Henkels. Claims 12-17 each recite combinations of features of independent claim 11 and hence claims 12-17 are not anticipated by Henkels for at least the above-stated reasons that claim 11 is not anticipated by Henkels.

Claims 2-7 and 12-17 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Henkels.

Applicants further assert that Henkels does not disclose "another inverter coupled between the bit line and an input of the latch" as recited in claim 2. The Examiner had previously cited element BL in Figure 1 of Henkels as disclosing the claimed bit line and previously cited elements 11 and 12 in Figure 1 of Henkels as disclosing the claimed latch. Office Action (11/1/2006), page 6. The Examiner further cites elements 55 and 56 of Figure 5 and column 4, lines 15-19 of Henkels as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

Henkels instead discloses that the PMOS FET 50 is controlled by the output of the inverter pair 55, 56. Column 4, lines 16-17. While Henkels discloses inverter pair 55, 56, inverter pair 55, 56, as illustrated in Figure 5, is not coupled between bit line BL (Examiner asserts that bit line BL of Henkels discloses the claimed bit line) and an input of elements 11 and 12 (Examiner asserts that elements 11 and 12 disclose the claimed latch). Thus, Henkels does not disclose all of the limitations of claim 2, and thus Henkels does not anticipate claim 2. M.P.E.P. §2131.

Applicants further assert that Henkels does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 3 and similarly in claim 13. The Examiner had previously cited elements 11 and 12 in Figure 1 of Henkels as disclosing the claimed latch. Office Action (11/1/2006), page 6. The Examiner further cites column 4, lines 20-25 of Henkels as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

As illustrated in Figure 1 of Henkels, the output of elements 11 and 12 is not an output of a register file. Thus, Henkels does not disclose all of the limitations of

claims 3 and 13, and thus Henkels does not anticipate claims 3 and 13. M.P.E.P. §2131.

Applicants further assert that Henkels does not disclose "wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter" as recited in claim 4. The Examiner had previously cited element 15 in Figure 1 of Henkels as disclosing the claimed inverter. Office Action (11/1/2006), page 6. The Examiner further cites column 4, lines 15-20 of Henkels as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

As illustrated in Figure 1, inverter 15 of Henkels is not a tri-state inverter. Neither does inverter 15 receive a hold select signal to control the operation of the inverter. Thus, Henkels does not disclose all of the limitations of claim 4, and thus Henkels does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that Henkels does not disclose "wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch" as recited in claim 5. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 5. M.P.E.P. §2131.

Applicants further assert that Henkels does not disclose "wherein data is read out of the register array to be input into the latch" as recited in claim 6 and similarly in claim 16. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not

established a *prima facie* case of anticipation in rejecting claims 6 and 16. M.P.E.P. §2131.

Applicants further assert that Henkels does not disclose "an inverter coupled between the bit line and an input of the latch" as recited in claim 12. Applicants further assert that Henkels does not disclose "wherein the transmission gate circuit receives a hold select signal" as recited in claim 14. Applicants further assert that Henkels does not disclose "wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled to the output of the latch" as recited in claim 15. The Examiner has not specifically addressed these limitations. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed these limitations, the Examiner has not established a *prima facie* case of anticipation in rejecting claims 12, 14 and 15. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Henkels, and thus claims 1-7 and 11-17 are not anticipated by Henkels. M.P.E.P. §2131.

II. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 1-20 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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